CLAIMS

1. A semiconductor device comprising:

a processor unit;

an internal interface section connected to said processor unit;

an external interface section connected to said processor unit and said internal interface section; and

a plurality of data processing units connected to said internal interface section,

wherein said processor unit comprises an internal CPU,

wherein said external interface section is connected to an external CPU, and

wherein each of said plurality of data processing units can be controlled by any one of said internal CPU and the external CPU, via said internal interface section.

2. The semiconductor device as defined in claim 1, wherein said internal interface section comprises:

a first bus connected to said processor unit;

a second bus connected to said external interface section; and

a plurality of selecting units, each of said plurality of selecting units being connected to said first bus and said second bus, and further connected to each of said plurality of data processing units in a one-to-one correspondence manner,

wherein each of said plurality of selecting units selects one of said first bus and said second bus as a bus to which each corresponding one of said plurality of data processing units is to be connected, and

wherein each of said plurality of data processing units can be controlled by any one of said internal CPU and the external CPU, via the bus selected by each corresponding one of said plurality of selecting units.

3. The semiconductor device as defined in claim 1, wherein said external interface section comprises:

a plurality of interface units connected to a plurality of external CPUs in a one-to-one correspondence manner, and

wherein each of said plurality of data processing units can be controlled by any one of said internal CPU and the plurality of external CPUs.

4. The semiconductor device as defined in claim 3, wherein said plurality of interface units include a first interface unit and a second interface unit, said first interface unit and said second interface unit being connected to the plurality of external CPUs in a one-to-one correspondence manner,

wherein said internal interface section comprises:

a first arbiter unit connected to said first interface unit and said processor unit;

a second arbiter unit connected to said second interface unit and said processor unit;

a first bus connected to said first arbiter unit;

a second bus connected to said second arbiter unit; and

a plurality of selecting units, each of said plurality of selecting units being connected to said first bus and said second bus, and further connected to each of said plurality of data processing units,

wherein said first arbiter unit arbitrates between said internal CPU and one of the plurality of external CPUs connected to said first interface unit, thereby connecting the arbitrated CPU to said first bus,

wherein said second arbiter unit arbitrates between said internal CPU and one of the plurality of external CPUs connected to said second interface unit, thereby connecting the arbitrated CPU to said second bus,

wherein each of said plurality of selecting units is connected to each of said plurality of data processing units and selects one of said first bus and said second bus as a bus to which each corresponding one of said plurality of data processing units is to be connected, and

wherein each of said plurality of data processing units can be controlled by any one of said internal CPU and the plurality of external CPUs connected to said external interface section, via the selected bus and one of said first arbiter unit and said second arbiter unit.

5. The semiconductor device as defined in claim 3, wherein said plurality of interface units include a first interface unit and a second interface unit, said first interface unit and said second interface unit being connected to the plurality of external CPUs in a one-to-one correspondence manner,

wherein said internal interface section comprises:

a first bus connected to said first interface unit;

a second bus connected to said second interface unit;

a third bus connected to said processor unit;

a plurality of first selecting units, each of said plurality of first selecting units being connected to said first bus and said third bus; and

a plurality of second selecting units, each of said plurality of second selecting units being connected to said second bus and said third bus,

wherein said plurality of data processing units include one or more data processing units belonging to a first processing group and one or more data processing units belonging to a second processing group,

wherein said one or more data processing units belonging to the first processing group are connected to said plurality of first selecting units in a one-to-one correspondence manner,

wherein said one or more data processing units belonging to the second processing group are connected to said plurality of second selecting units in a one-to-one correspondence manner,

wherein each of said plurality of first selecting units selects one of said first bus and said third bus as a bus to which each corresponding one of the data processing

units belonging to the first processing group is to be connected,

wherein each of said plurality of second selecting units selects one of said second bus and said third bus as a bus to which each corresponding one of the data processing units belonging to the second processing group to be connected,

wherein each of said one or more data processing units belonging to the first processing group can be controlled by any one of said internal CPU and one of the plurality of external CPUs connected to said first interface unit, via the bus selected by each corresponding one of said plurality of first selecting units, and

wherein each of said one or more data processing units belonging to the second processing group can be controlled by any one of said internal CPU and one of the plurality of external CPUs connected to said second interface unit, via the bus selected by each corresponding one of said plurality of second selecting units.

6. The semiconductor device as defined in claim 3, wherein said plurality of interface units include a first interface unit and a second interface unit, said first interface unit and said second interface unit being connected to the plurality of external CPUs in a one-to-one correspondence manner,

wherein said internal interface section comprises:

an arbiter unit connected to said processor unit and said second interface unit;

a first bus connected to said first interface unit;

a second bus connected to said arbiter unit;

a third bus connected to said processor unit; and

a plurality of selecting units connected to said first bus and said third bus,

wherein said plurality of data processing units include one or more data processing units belonging to a first processing group and one or more data processing units belonging to a second processing group,

wherein said one or more data processing units belonging to the first processing group are connected to said plurality of selecting units in a one-to-one

correspondence manner,

wherein said one or more data processing units belonging to the second processing group are connected to said second bus,

wherein each of said plurality of selecting units selects one of said first bus and said third bus as a bus to which each corresponding one of said plurality of data processing units is to be connected,

wherein said arbiter unit arbitrates between said internal CPU and one of the plurality of external CPUs connected to said second interface unit, thereby connecting the arbitrated CPU to said second bus,

wherein each of said one or more data processing units belonging to the first processing group can be controlled by any one of said internal CPU and one of the plurality of external CPUs connected to said first interface unit, via the bus selected by each corresponding one of said plurality of selecting units, and

wherein each of said one or more data processing units belonging to the second processing group can be controlled by any one of said internal CPU and one of the plurality of external CPUs connected to said second interface unit, via said arbiter unit and said second bus.

7. The semiconductor device as defined in claim 1, wherein said processor unit comprises a plurality of internal CPUs, and

wherein each of said plurality of data processing units can be controlled by any one of said plurality of internal CPUs and the external CPU.

8. The semiconductor device as defined in claim 7, wherein said plurality of internal CPU comprises:

a first internal CPU; and

a second internal CPU,

wherein said internal interface section comprises:

an arbiter unit connected to said first internal CPU and said second internal

CPU;

a first bus connected to said arbiter unit;

a second bus connected to said external interface section; and

a plurality of selecting units, each of said plurality of selecting units being connected to said first bus and said second bus, and further connected to each of said plurality of data processing units in a one-to-one corresponding manner,

wherein each of said plurality of selecting units selects one of said first bus and said second bus as a bus to which each corresponding one of said plurality of data processing units is to be connected,

wherein said arbiter unit arbitrates between said first internal CPU and said second internal CPU, thereby connecting the arbitrated CPU to said first bus, and

wherein each of said plurality of data processing units can be controlled by any one of said first internal CPU, said second internal CPU, and said external CPU, via a bus selected by each corresponding one of said plurality of selecting units.

9. The semiconductor device as defined in claim 7, wherein said plurality of internal CPU comprises:

a first internal CPU; and

a second internal CPU,

wherein said internal interface section comprises:

a switching unit connected to said first internal CPU and said second internal CPU;

a first bus connected to said switching unit;

a second bus connected to said external interface section; and

a plurality of selecting units, each of said plurality of selecting units being connected to said first bus and said second bus, and further connected to each of said plurality of data processing units in a one-to-one corresponding manner,

wherein each of said plurality of selecting units selects one of said first bus

and said second bus as a bus to which each corresponding one of said plurality of data processing units is to be connected,

wherein said switching unit switches between said first internal CPU and said second internal CPU, thereby connecting the switched CPU to said first bus, and

wherein each of said plurality of data processing units can be controlled by any one of said first internal CPU, said second internal CPU, and said external CPU, via the bus selected by each corresponding one of said plurality of selecting units.

10. The semiconductor device as defined in claim 7, wherein said plurality of internal CPU comprises:

a first internal CPU; and

a second internal CPU,

wherein said internal interface section comprises:

a first arbiter unit to said first internal CPU and said external interface section;

a second arbiter unit connected to said second internal CPU and said external interface section;

a first bus connected to said first arbiter unit; and

a second bus connected to said second arbiter unit,

wherein said plurality of data processing units include one or more data processing units belonging to a first processing group and one or more data processing units belonging to a second processing group,

wherein said one or more data processing units belonging to the first processing group are connected to said first bus,

wherein said one or more data processing units belonging to the second processing group are connected to said second bus,

wherein said first arbiter unit arbitrates between said first internal CPU and the external CPU connected to said external interface section, thereby connecting the arbitrated CPU to said first bus,

wherein said second arbiter unit arbitrates between said second internal CPU and the external CPU connected to said external interface section, thereby connecting the arbitrated CPU to said second bus,

wherein each of the data processing units belonging to the first processing group can be controlled by any one of said first internal CPU and the external CPU, via said first arbiter unit and said first bus, and

wherein each of the data processing units belonging to the second processing group can be controlled by any one of said second internal CPU and the external CPU, via said second arbiter unit and said second bus.

11. The semiconductor device as defined in claim 7, wherein said plurality of internal CPU comprises:

a first internal CPU; and

a second internal CPU,

wherein said internal interface section comprises:

a first bus connected to said first internal CPU;

a second bus connected to said second internal CPU;

a third bus connected to said external interface section;

a plurality of first selecting units connected to said first bus and said third bus; and

a plurality of second selecting units connected to said second bus and said third bus,

wherein said plurality of data processing units include one or more data processing units belonging to a first processing group and one or more data processing units belonging to a second processing group,

wherein said one or more data processing units belonging to the first processing group are connected to said plurality of first selecting units in a one-to-one correspondence manner,

wherein said one or more data processing units belonging to the second processing group are connected to said plurality of second selecting units in a one-to-one correspondence manner,

wherein each of said plurality of first selecting units selects one of said first bus and said third bus as a bus to which each corresponding one of said data processing units belonging to the first processing group is to be connected,

wherein each of said plurality of second selecting units selects one of said second bus and said third bus as a bus to which each corresponding one of said data processing units belonging to the second processing group is to be connected,

wherein each of said one or more data processing units belonging to the first processing group can be controlled by any one of said first internal CPU and the external CPU connected to said external interface section, via the bus selected by the corresponding one of said plurality of first selecting units, and

wherein each of said one or more data processing units belonging to the second processing group can be controlled by any one of said second internal CPU and the external CPU connected to said external interface section, via the bus selected by the corresponding one of said plurality of second selecting units.

12. The semiconductor device as defined in claim 1, wherein said processor unit comprises a plurality of internal CPUs,

wherein said external interface section comprises a plurality of interface units,

wherein said plurality of interface units are connected to a plurality of external CPUs in a one-to-one correspondence manner, and

wherein each of said plurality of data processing units can be controlled by any one of said plurality of internal CPUs and the plurality of external CPUs.

13. The semiconductor device as defined in claim 12, wherein said plurality of internal CPUs comprises:

a first internal CPU; and

a second internal CPU,

wherein said plurality of interface units comprises:

a first interface unit; and

a second interface unit,

wherein said first interface unit and said second interface unit are connected to the plurality of external CPUs in a one-to-one correspondence manner,

wherein said internal interface section comprises:

a first bus connected to said first internal CPU;

a second bus connected to said first interface unit;

a third bus connected to said second internal CPU;

a fourth bus connected to said second interface unit;

a plurality of first selecting units connected to said first bus and said second bus; and

a plurality of second selecting units connected to said third bus and said fourth bus,

wherein said plurality of data processing units include one or more data processing units belonging to a first processing group and one or more data processing units belonging to a second processing group,

wherein said one or more data processing units belonging to the first processing group are connected to said plurality of first selecting units in a one-to-one corresponding manner,

wherein said one or more data processing units belonging to the second processing group are connected to said plurality of second selecting units in a one-to-one corresponding manner,

wherein each of said plurality of first selecting units selects one of said first bus and said second bus as a bus to which each corresponding one of said one or more data processing units belonging to the first processing group is to be connected,

wherein each of said plurality of second selecting units selects one of said third bus and said fourth bus as a bus to which each corresponding one of said one or more data processing units belonging to the second processing group is to be connected,

wherein each of said one or more data processing units belonging to the first processing group can be controlled by any one of said first internal CPU and the external CPU connected to said first interface unit, via the bus selected by each corresponding one of said plurality of first selecting units, and

wherein each of said one or more data processing units belonging to the second processing group can be controlled by any one of said second internal CPU and the external CPU connected to said second interface unit, via the bus selected by each corresponding one of said plurality of second selecting units.

14. The semiconductor device as defined in claim 1, wherein said internal CPU included in said processor unit and the external CPU connected to said external interface section operate in parallel.

15. The semiconductor device as defined in claim 7, wherein each of said plurality of internal CPUs included in said processor unit operates at a variable operating frequency.

16. The semiconductor device as defined in claim 1, wherein said plurality of data processing units include at least two of a moving picture processing circuit, a graphics processing circuit, a still picture processing circuit, a voice/audio processing circuit, a video input/output circuit, and a voice/audio input/output circuit.

17. A mobile phone comprising:

said semiconductor device as defined in claim 1;

an application processing LSI;

a RF processing LSI; and

a baseband processing LSI,

wherein said semiconductor device executes video data processing and audio data processing that require high load when executed by said application processing LSI.

18. The mobile phone as defined in claim 17, wherein said application processing LSI comprises at least one or more CPUs operable to share processing of the CPU included in said semiconductor device.